REMARKS

This is a full and complete response to the Office Action, dated October 25, 2010.

In the aforementioned Office Action, the Examiner noted that claims 1, 2, and 4-20 are pending, that claims 1, 2, 4-7 and 9-20 stand rejected under 35 U.S.C. §102(b) as anticipated by Henrion (U.S. Patent 5,461,615), and that claim 8 is allowed.

In view of the following remarks, it is submitted that the claims pending in the application are novel and nonobvious. It is believed that this application is in condition for allowance. By this response, reconsideration of the present application is respectfully requested.

Allowable Subject Matter

Assignee thanks the Examiner for allowing claim 8. However, Assignee points out that this claim merely sets forth examples of allowable subject matter and that other claims supported by the disclosure of this application, including the remaining pending claims, are also allowable.

35 U.S.C. § 102(b) Rejection

Claims 1, 2, 4-7, and 9-20 stand rejected under 35 U.S.C. §102(b) as anticipated by Henrion (U.S. Patent 5,461,615). This rejection is respectfully traversed.

To anticipate a claim under §102, the applied document must teach each and every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." [MPEP §2131.01] Henrion does not teach each and every element of the rejected claims.

Claim 1, for example, recites:

A method for assigning an address to a node in a network having an arbitrary topology, the method comprising:

assigning a first address to a first node such that the first address includes a description of a path to the first node;

assigning a second address to the first node such that the second address includes a description of another path to the first node; and

establishing a mapping between a plurality of output ports in the network and bits in the first or second address such that a packet, directed to the first node, at a second node in the network is forwarded via an output port on the second node in the network, in response to a specified bit in the first or second address having a specified value.

The Examiner rejects claim 1 by asserting that Henrion teaches assigning a first address to a first node such that the first address includes a description of a path to the first node, and assigning a second address to the first node such that the second address includes a description of another path to the first node. To make such an assertion, the Examiner relies on Henrion teaching a first set of three bits describing a path ***to the first node*** and a second set of three bits describing ***another path to the first node***. Assignee respectfully disagrees and submits that Henrion fails to teach describing paths to the first node. For example, Henrion's first set of three bits and second set of three bits each apparently comprise an identification of one ***output of the node***, as the Examiner notes (also see Henrion, col. 8, lines 20-23). Identifying an output of a node, however, is not the same as identifying or describing ***a path to the node***, as set forth in claim 1. Referring to Henrion, column 8, lines 20-25, for example, a difference between 'identifying an output of a node' and 'describing a path to the node' may be shown, as follows.

Each of the three bit sets in an address of Henrion apparently identifies an output of switching elements S11, S21, and S38, respectively. Referring to FIG. 2, Henrion's address (the group of three bit sets) may be used to find a routing path of a packet from an input port of an input switching element to an output port of an output switching element. In other words, Henrion's address is able to describe a required routing path of the packet. However, it is not possible to determine a correct routing path for a packet to pass through the switching elements if only one of the three bit sets is given. Hence, 'identifying an output of a node' is not the same as 'describing a path to the node'. Henrion's bit sets cannot be considered as addresses. Thus, Henrion does not show ***assigning a first address to a first node such that the first address includes a description of a path to the first node and***

assigning a second address to the first node such that the second address includes a description of another path to the first node, as set forth in claim 1.

Instead of teaching, among other things, describing a path to a switching element or node, as set forth in claim 1, Henrion teaches "...a plurality of sets of bits each identifying one output of a switching element through which the cell must pass" (col. 8, lines 12-15 and lines 20-27). Referring to Henrion, FIG. 2, for example, an address or description of an output of switching element S38 apparently comprises a first set of three bits, a second set of three bits, and a third set of five bits (col. 8, lines 20-25). In Henrion's example, there are three switching elements, S11, S21, and S38, in a ***single path*** to output OP2048. The first set of three bits identifies one output of S11 along the single path, the second set of three bits identifies one output of S21 along ***the same single path***, and the third set of five bits identifies one output of S38 along the same single path. Though each set of bits identifies an output along ***the same single path***, the Examiner, on page 2, lines 16-21 of the Office Action, asserts that Henrion's first set of three bits describes one path and Henrion's second set of three bits describes another path. But, as explained above, this is not the case. The Assignee respectfully submits that Henrion does not teach assigning a first and a second address to a first node such that the first address includes a description of a path to the first node and the second address includes a description of another path to the first node, as set forth in claim 1. Also, Henrion's network nodes are limited to being assigned a single address to describe ***a single particular path*** from a beginning node. Again, Henrion does not teach describing more than one path to a node, as set forth in claim 1.

Pointing to FIG. 2 and column 8, lines 12-35 of Henrion, the Examiner asserts that Henrion teaches establishing a mapping between a plurality of output ports in the network and bits in the first or second address such that a packet, directed to the first node, at a second node in the network is forwarded via an output port on the second node in the network, in response to a specified bit in the first or second address having a specified value. The Assignee respectfully disagrees. While Henrion may show routing a data packet (or cell) along a single network path described by an internal routing label or address of a node, Assignee submits that Henrion is limited to a single, unique address for each node. For example, referring to FIG. 2 of Henrion, if a data cell entering network SN1 at input IP1 is addressed to node OP2048, then the data cell will apparently travel a particular path to node OP2048, as discussed above. Because Henrion

does not teach a network node having more than one address to describe the node's location, any data cell addressed to node OP2048 and starting at input IP1, for example, will apparently travel the same particular path. In other words, Henrion's network nodes are limited to being assigned a single address to describe a single particular path from a beginning node.

Accordingly, Henrion fails to teach ***establishing a mapping between a plurality of output ports in the network and bits in the first or second address such that a packet, directed to the first node, at a second node in the network is forwarded via an output port on the second node in the network***, in response to a specified bit in the first or second address having a specified value, as set forth in claim 1. Therefore, since Henrion does not teach or suggest each and every limitation of claim 1, Assignee requests withdrawal of the rejection of this claim under 35 USC 102(b). It is respectfully asserted that claim 1 covers patentable subject matter. Favorable action in this regard is respectfully requested.

Claims 2, and 4-7, depend from claim 1 and include all of the limitations of claim 1. It is therefore respectfully asserted that these claims also patentably distinguish from Henrion on at least the same basis as claim 1. Therefore, it is also respectfully asserted that these claims cover patentable subject matter and favorable action in this regard is also respectfully requested.

The remaining independent claims, 9, 11, 15, and 19, although not identical in scope with claim 1, are believed to patentably distinguish from Henrion on at least a similar basis as claim 1. Accordingly, Assignee respectfully requests withdrawal of the rejection of these claims and early allowance. Assignee respectfully also submits that claims 10, 12-14, 16-18, and 20 patentably distinguish over Henrion on at least the same basis as the independent claims from which they respectively depend. Accordingly, Assignee respectfully requests withdrawal of the rejection of dependent claims 10, 12-14, 16-18, and 20 under 35 U.S.C. § 102(b) and allowance as well.

It is noted that claimed subject matter may be patentably distinguished from the applied document for additional reasons; however, the foregoing is believed to be sufficient to overcome the Examiner's rejections discussed above.

Further, it is noted that the Assignee's failure to comment directly upon any positions asserted by the Examiner in the office action does not indicate agreement or acquiescence with those asserted positions. Rather, it is believed that the foregoing remarks render moot positions not commented upon directly. Accordingly, Assignee reserves the right to pursue additional claims that may be broader in scope than the pending claims in a filing that claims priority to this patent application.

CONCLUSION

In view of the foregoing, it is respectfully submitted that all the claims pending in this patent application are in condition for allowance. Reconsideration and allowance of all the claims are respectfully solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Brian D. Wichner at (503) 439-6500 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

In the event there are any errors with respect to the fees for this response or any other papers related to this response, the Director is hereby given permission to charge any shortages and credit any overcharges of any fees required for this submission to Deposit Account No. 50-3130.

Respectfully submitted,

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